TEST MODE CIRCUIT OF SEMICONDUCTOR MEMORY DEVICE

BACKGROUND OF THE INVENTION

1. Background of the Invention

[0001] The present invention relates to test mode circuits of semiconductor memory devices, and more specifically, to a test mode circuit of a semiconductor memory device which reduces the number of metal lines used for selecting a test mode item by grouping the test mode items.

2. Description of the Prior Art

[0002] Fig. 1 is a block diagram illustrating a conventional test mode circuit of a semiconductor memory device.

[0003] The conventional test mode circuit comprises a test mode controller 1, an address decoder 2 and a test mode decoder 3.

[0004] The test mode controller 1 is controlled by a mode register set signal MRS, and outputs a test mode setting signal TMS and a test mode end signal TME for setting a test mode depending on states of an address signal ADD<7>.

[0005] The mode register set signal MRS is generated at a rising edge of an inputted clock signal when a row address strobe signal /RAS, a column address strobe signal /CAS, a chip selecting signal /CS and a write enable signal /WE are

simultaneously at a low level (not shown).

[0006] The address decoder 2 decodes address signals ADD<0:5>, and outputs decoding address signals TMADD<0:63> for selecting each test mode item. Here, a test mode circuit using 64 test mode items is exemplified. Accordingly, the decoding address signal TMADD<0:63> of 64 bits obtained by decoding the address signal ADD<0:5> of 6 bits is used to select each test mode item.

[0007] The test mode decoder 3 is controlled by the test mode setting signal TMS and the test mode end signal TME, and selects each test mode item in response to the decoding address signals TMADD<0:63>. The test mode decoder 3 activates corresponding test mode item selecting signals TM<0:63> to select a specific test mode item so that a test may be performed using the specific test mode item.

[0008] Fig. 2 is a circuit diagram illustrating the test mode controller 1 of Fig. 1.

[0009] The test mode controller 1 comprises NAND gates NDS and NDE, and inverters INS and INE. The NAND gate NDS performs a NAND operation on the mode register set signal MRS and the address signal ADD<7>. The inverter INS inverts an output signal from the NAND gate NDS, and outputs the test mode setting signal TMS. The NAND gate NDE performs a NAND operation on the mode register set signal MRS and an inverted

address signal /ADD<7> outputted by the inverter INV. The inverter INE inverts an output signal from the NAND gate NDE, and outputs the test mode end signal TME.

[0010] Fig. 3 is a circuit diagram illustrating the address decoder 2 of Fig. 1.

[0011] The address decoder 2 comprises inverters INV0~INV5, NAND gates ND10~ND163, and inverters INV10~INV163. The inverters INV0~INV5 invert address signals ADD<0:5>, respectively. The NAND gates ND10~ND163 perform NAND operations on address signals ADD<0:5> and output signals from the inverters INV0~INV5. The inverters INV10~INV163 invert output signals from the NAND gates ND10~ND163, and output decoding address signals TMADD<0:63>.

[0012] Fig. 4 is a circuit diagram illustrating the test mode decoder 3 of Fig. 1.

[0013] The test mode decoder 3 comprises 64 test mode item selecting means 4. The test mode item selecting means 4 is controlled by the test mode setting signal TMS and the test mode end signal TME, and outputs test mode item selecting signals TM<0:63> for selecting each test mode item in response to the decoding address signals TMADD<0:63>.

[0014] Each test mode item selecting means 4 comprises a PMOS transistor PM1, NMOS transistor NM1 and NM2, and a latch 5. The PMOS transistor PM1 has a gate to receive the test mode

end signal TME. The NMOS transistor NM1 has a gate to receive the test mode setting signal TMS. The NMOS transistor NM2 has a gate to receive a corresponding signal of the decoding address signals TMADD<0:63>. The latch 5 is connected to a common drain of the PMOS transistor PM1 and the NMOS transistor NM1. The latch 5 comprises inverters INL1 and INL2. An output signal from the inverter INL1 is inputted to an input terminal of the inverter INL2, and an output signal from the inverter INL2 is inputted to an input terminal of the inverter INL1.

[0015] Next, the operation of the conventional test mode circuit is described.

[0016] If a system is activated when the mode register set signal MRS transitions to a high level, a test mode is set depending on the state of the address signal ADD<7>.

[0017] If the address signal ADD<7> is at a high level, the test mode setting signal TMS transitions to a high level to activate the test mode.

[0018] When one of the decoding address signals TMADD<0:63> transitions to a high level, a test mode item selecting signal outputted from the corresponding test mode item selecting means 4 is enabled to a high level.

[0019] Thereafter, a test circuit corresponding to the activated test mode item selecting signal sets a test mode,

and is prepared to perform a test.

[0020] In the conventional test mode circuit, the peripheral circuit region is enlarged because a corresponding metal line is required for setting each test mode item. As a result, cell efficiency is degraded.

SUMMARY OF THE INVENTION

[0021] Accordingly, it is an object of the present invention to provide a test mode circuit comprising a group having a predetermined number of test mode items to reduce the number of metal lines associated with the circuit.

[0022] In an embodiment of the present invention, there is provided a test mode circuit of a semiconductor memory device comprising a test mode controller, a test mode decoder and a test mode item selecting means. The test mode controller outputs a test mode setting signal to control a test mode setting operation in response to a mode register set signal and an address signals which are used in setting a test mode. The test mode decoder, controlled by the test mode setting signal, selects a test mode item group in response to upper address bits of the address signal. The test mode item selecting means selects a predetermined test mode item of the test mode item group selected by the test mode decoder in response to lower address bits of the address signal. The test

mode item group includes a predetermined number of test mode items among a plurality of test mode items as a unit.

BRIEF DESCRIPTION OF THE DRAWINGS

[0023] Fig. 1 is a block diagram illustrating a conventional test mode circuit of a semiconductor memory device.

[0024] Fig. 2 is a circuit diagram illustrating a test mode controller of Fig. 1.

[0025] Fig. 3 is a circuit diagram illustrating an address decoder of Fig. 1.

[0026] Fig. 4 is a circuit diagram illustrating a test mode decoder of Fig. 1.

[0027] Fig. 5 is a block diagram illustrating a test mode circuit of a semiconductor memory device according to an embodiment of the present invention.

[0028] Fig. 6 is a circuit diagram illustrating a test mode decoder of Fig. 5.

[0029] Fig. 7 is a circuit diagram illustrating a test mode item selecting signal generator of Fig. 5.

[0030] Fig. 8 is a block diagram illustrating a test mode circuit of a semiconductor memory device according to another embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0031] The present invention will be described in detail with reference to the attached drawings.

[0032] Fig. 5 is a block diagram illustrating a test mode circuit of a semiconductor memory device according to an embodiment of the present invention.

[0033] In an embodiment, the test mode circuit comprises a test mode controller 10, a first address decoder 20, a test mode decoder 30, a second address decoder 40 and a test mode item selecting means 50.

[0034] The test mode controller 10 is controlled by a mode register set signal MRS, and outputs a test mode setting signal TMS and a test mode end signal TME for setting a test mode depending on states of an address signal ADD<7>.

[0035] The first address decoder 20 decodes address signals ADD<0:3>, and outputs decoding address signals TMADD<0:15> for selecting each test mode item group.

[0036] The test mode decoder 30 is controlled by the test mode setting signal TMS and the test mode end signal TME, and outputs test mode item group selecting signals TMDEC<0:15> for selecting each test mode item group in response to the decoding address signals TMADD<0:15>.

[0037] The second address decoder 40 decodes address signals ADD<4:5>, and outputs decoding address signals ADDDEC<0:3> for

selecting a desired test mode item of the selected test mode item group.

[0038] The test mode item selecting means 50 outputs test mode item selecting signals TM<0:63> for selecting a desired test mode item in response to the decoding address signals ADDDEC<0:3> of the test mode item group selected by the test mode item group selecting signals TMDEC<0:15>.

[0039] Fig. 6 is a circuit diagram illustrating the test mode decoder 30 of Fig. 5.

[0040] The test mode decoder 30 comprises 16 test mode item selecting means 31. The test mode item selecting means 31 are controlled by the test mode setting signal TMS and the test mode end signal TME, and output the test mode item group selecting signals TMDEC<0:15> for selecting each test mode item group in response to the decoding address signals TMADD<0:15>.

[0041] Each test mode item selecting means 31 comprises a PMOS transistor PM11, NMOS transistors NM11 and NM12, and a latch 32. The PMOS transistor PM11 has a gate to receive the test mode end signal TME. The NMOS transistor NM11 has a gate to receive the test mode setting signal TMS. The NMOS transistor NM12 has a gate to receive a corresponding signal of the decoding address signals TMADD<0:15>. The latch 32 is connected to a common drain of the PMOS transistor PM11 and

the NMOS transistor NM11. The latch 32 comprises inverters INL11 and INL12. An output signal from the inverter INL11 is inputted to an input terminal of the inverter INL12, and an output signal from the inverter INL12 is inputted to an input terminal of the inverter INL11.

[0042] Fig. 7 is a circuit diagram illustrating the test mode item selecting means 50 of Fig. 5.

[0043] The test mode item selecting means 50 comprises 16 unit selecting means 51. The unit selecting means 51 output test mode item selecting signals TM<0:63> for selecting a desired test mode item of the test mode item group selected by the test mode item group selecting signal TMDEC<0:15> in response to the decoding address signals ADDDEC<0:3>.

[0044] The unit selecting means 51 comprises NAND gates ND21~ND24, and inverters INV21~INV24. The NAND gates ND21~ND24 perform NAND operations on the decoding address signals ADDEC<0:3> and a corresponding signal of the test mode item group selecting signals TMDEC<0:15>. The inverters INV21~INV24 invert output signals from the NAND gates ND21~ND24, and output the test mode item selecting signals TM<0:63>.

[0045] The explanation of the address decoders 20 and 40 is omitted because conventional decoder circuits such as described above are used therein.

[0046] Next, the operation of the test mode circuit according

to an embodiment of the present invention is described.

[0047] If a system is activated when the mode register set signal MRS transitions to a high level in the test mode controller 10, the state of a test mode is set depending on the state of the address signal ADD<7>.

[0048] For example, if the address signal ADD<7> is at a high level, the test mode setting signal TMS transitions to a high level to enable the test mode.

[0049] Here, if a desired signal of the decoding address signals TMADD<0:15> transitions to a high level to select a desired test mode item group in the test mode decoder(30), a corresponding signal of the test mode item group selecting signals TMDEC<0:15> is enabled to a high level.

[0050] If a desired signal among the decoding address signals ADDDEC<0:3> transitions to a high level to select a desired test mode item in the test mode item selecting means 50, a desired signal among the test mode item selecting signals TM<0:63> is activated because the unit selecting means 51 corresponding to a signal enabled to a high level among the test mode item group selecting signals TMDEC<0:15> is already activated.

[0051] As a result, a corresponding test circuit sets a test mode, and is prepared to perform a test.

[0052] Fig. 8 is a block diagram illustrating a test mode

circuit of a semiconductor memory device according to another embodiment of the present invention. Here, a test mode circuit selecting 16 test mode items is exemplified.

[0053] In an embodiment of the present invention, the test mode circuit comprises a test mode controller 10, a test mode decoder 30 and a test mode item selecting means 50.

[0054] The test mode decoder 30 is controlled by a test mode setting signal TMS and a test mode end signal TME, and outputs test mode item group selecting signals TMDEC<0:3> for selecting each test mode item group in response to address signals ADD<0:3>.

[0055] The test mode item selecting means 50 outputs test mode item group selecting signals TM<0:15> for selecting a desired test mode item out of the test mode item group selected by the test mode item group selecting signals TMDEC<0:3> in response to address signals ADD<4:8>.

[0056] Here, the explanation on the operation of the test mode circuit of Fig. 8 is omitted because it is identical to that of Fig. 5.

[0057] In the test mode circuit of Fig. 8, the address decoders 20 and 40 of Fig. 5 are not used. Instead, the address signals ADD<0:3> are directly inputted to the test mode decoder 30, and the address signals ADD<4:8> are directly inputted to the test mode item selecting means 50. When

compared with that of Fig. 5, the test mode circuit of Fig. 8 does not require the address decoders 20 and 40. As a result, the configuration of the circuit can be simplified.

[0058] Accordingly, in a test mode circuit of a semiconductor memory device according to an embodiment of the present invention, the number of metal lines can be reduced because the test mode circuit having a group comprising a predetermined number of test mode items selects a test mode item group.

[0059] While the present invention is susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and described in detail herein. However, it should be understood that the invention is not limited to the particular forms disclosed. Rather, the invention covers all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined in the appended claims.